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10/633,362	08/04/2003	Wilco Dijkstra	550-455	5128

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EXAMINER	
MOLL, JESSE R	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 09/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,362	DIJKSTRA, WILCO	
	Examiner	Art Unit	
	Jesse R. Moll	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
9/17/2006

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-42 have been examined.

Acknowledgment of papers filed: amendment on 7 July, 2006. The papers filed have been placed on record.

Drawings

The drawings were received on 7 July 2006. These drawings are accepted.

Withdrawn Objections / Rejections

2. Applicant, via amendment has overcome the objection to the title. Therefore, the objection has been respectfully withdrawn.

3. Applicant, via amendment has overcome the objections to Claims 15 and 35-39. The objections have been respectfully withdrawn.

4. Applicant, via amendment has overcome the rejections of Claims 1 and 22 under 35 U.S.C. §112 second paragraph. The rejections have been respectfully withdrawn.

Claim Objections

5. Examiner request the duplicate "together" be removed on line 9.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

7. Claims 1-42 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant Admitted Prior Art (figs. 1-5; Description of the Prior Art; pages 1-5).

8. Referring to claim 1, Applicant discloses a data processing apparatus (processing apparatus 5; see fig. 1; page 1, line 7) comprising: a processor core (processor core 10; see fig. 1; page 1, line 8) operable to process a sequence of instructions (see page 1, line 8), said processor core having a plurality of pipeline stages (see fig. 2; page 1, lines 22-23), one of said plurality of pipeline stages being an address generation stage (second execution stage 90; see fig. 2; page 2, lines 10-11) operable to generate an address (see page 2, lines 10-11) associated with an instruction (instruction causing memory access; see page 2, lines 6-7) for subsequent processing by said pipeline stages (memory stage 100; see page 1, last line; page 2, first line), said instruction being one from a first group of instructions (all LDR

instructions (a - e); see page 2 lines 14-29 and page 3, lines 1-3) or a second group of instructions (LDR instructions which require a shift operation (d & e); see page 2, last 3 lines and page 3, lines 1-3;

Note that the first group comprises the second group and all other load instructions.),

said address generation stage comprising: address generation logic (ADD unit 170; see page 5, lines 1-3) for receiving operands (x and y; see fig 3B; page 3, lines 13-14 and 20-21) associated with said instruction (instructions a-d contain registers Rb and Rc; see page 2, lines 21-29), for generating a shifted operand (multiplexer 130 generates shifted operand;

Note that the definition of generate according to The Free On-line Dictionary of Computing, © 1993-2005 Denis Howe is "To produce something according to an algorithm or program or set of rules, or as a (possibly unintended) side effect of the execution of an algorithm or program." Using this definition, multiplexer 130 produces either input at the output. Therefore, it is possible for multiplexer 130 to produce/generate the shifted value that is output by SHIFT unit 135.)

from one of said operands (X; see page 3, lines 16-17), and for adding together, in dependence on said instruction (see page 3, lines 23-24), a register selected ones from said operands (Y; see fig. 3b; page 3, lines 20-21) and said shifted operand (see fig. 3B; page 3, lines 14-18;

Note that either the shifted value of X or X can be sent to input B of adder 170 by multiplexer 137. If the instruction requires a shift, the adder receives the shifted value; otherwise, it receives X.)

to generate said address for subsequent processing by said pipeline stages (see page 2, lines 10-11); and operand routing logic (multiplexers 155 and 165; see fig. 5), in dependence on said instruction (depending which type of instruction it is), for routing operands associated with instructions (operand X) from said first group of instructions to said address generation logic (see page 4, lines 28-30;

Note that not all instructions are routed. Only load or store instructions requiring shifting are routed.)

and for routing operands associated with instructions (operand X) from said second group of instructions via operand manipulation logic (shifter 160; see fig. 4; page 4, lines 27-28) for manipulation of said operands (shift unit 160 shifts data) prior to routing to said address generation logic (see page 4, lines 4-6).

Further note that claim 22 recites equivalent limitations as claim 1 and is rejected under the same grounds. If the apparatus disclosed performs these actions, there must be a method it uses. This method anticipates claim 22.

9. Regarding claim 2, Applicant discloses the data processing apparatus of claim 1, wherein said instruction relates to a memory access and said address indicates a location in memory to be accessed (see page 2, lines 14-20).

10. Regarding claim 3, Applicant discloses the data processing apparatus of claim 1, wherein said first group of instructions comprises a first instruction (any non-shift LDR) which causes the processor core to logically add together two operands (added by ADD unit 140; see above regarding claim 1), and a second instruction (any LDR requiring a shift) which causes the processor core to logically add together one operand to another operand (added by ADD unit 140; see above regarding claim 1) logically shifted by one of a predetermined number of bits (see page 2, lines 27-29;

Note that the number of bits is determined when the code is written before it is executed, and is therefore predetermined.).

11. Regarding claim 4, Applicant discloses the data processing apparatus of claim 3, wherein said address generation logic is operable to generate said another operand logically shifted by one of a predetermined number of bits (multiplexer 130 can generate X; see page 3, lines 13-15; see above regarding claim 1).

12. Regarding claim 5, Applicant discloses the data processing apparatus of claim 3, wherein said second instruction causes the processor core to logically add together one operand (see page 3, lines 23-24) to another operand logically shifted left by two bits (see page 3, line 19-20;

Note that the operand can be shifted from 1 to 31 bits. It therefore can be shifted by two bits.).

13. Regarding claim 6, Applicant discloses the data processing apparatus of claim 5, wherein said address generation logic is operable to generate said another operand logically shifted left by two bits (the 2-bit shifted value is generated by multiplexer 130; see above regarding claims 1 and 5).

14. Regarding claim 7, Applicant discloses the data processing apparatus of claim 3, wherein said second instruction causes the processor core to logically add together one operand to another operand (see above regarding claim 5) subject to only one preset logical shift operation (shift done by SHIFT unit 160;

Note that the only shift done to the two operands is by SHIFT unit 160.).

15. Regarding claim 8, Applicant discloses the data processing apparatus of claim 1, wherein said address generation logic is operable to perform only one predetermined logical shift operation (see above regarding claim 7;

Note that the shift operation is predetermined because the number of bits shifted is hard coded into the program and is determined before execution.)

and operands (X and Y; see page 3, lines 13-16 and 20-21) associated with all other logical shift operations required by instructions from said second group of instructions (any LDR requiring a shift; see page 2, lines 27-29) are routed via operand manipulation logic (SHIFT unit 160; see page 5, lines 1-3) for manipulation of operands (shift unit 160 shifts data) prior to routing to said address generation logic (see page 4, lines 4-6).

16. Regarding claim 9, Applicant discloses the data processing apparatus of claim 3, wherein said second group of instructions comprises instructions which cause the processor core to logically add together one operand to another operand (see page 3, lines 23-24) subject to any other logical shift operation (LDR instructions which require a shift operation (d & e); see page 4, last 3 lines and page 5, lines 1-3;

Note that any instruction which requires a shift operation will shift instructions by a number other than zero.).

17. Regarding claim 10, Applicant discloses the data processing apparatus of claim 9, wherein said operand manipulation logic is operable, in dependence on said instruction, to generate said another operand logically shifted by any other number of bits (LDR instructions which require a shift operation (d & e); page 4, last 3 lines and page 5, lines 1-6).

18. Regarding claim 11, Applicant discloses the data processing apparatus of claim 1, wherein said second group of instructions comprises instructions which cause the processor core to logically subtract one operand from another operand (instruction e; see page 3, lines 1-3).

19. Regarding claim 12, Applicant discloses the data processing apparatus of claim 11, wherein said operand manipulation logic is operable, in dependence on said

instruction (if the instruction is a subtraction operation), to generate an inverse representation of one of said operand and said another operand (see col. 3, lines 13-16;

Note that the inverter is considered to be part of the manipulation logic and not part of the address generation logic.).

20. Regarding claim 13, Applicant discloses the data processing apparatus of claim 1, wherein said second group of instructions comprises a subtractive instruction for which said address is generated by subtracting a subtrahend operand (Rc) from a minuend operand (Rb) associated with said instruction (instruction e; see page 3, lines 1-3), and said operand manipulation logic comprises subtraction operand generation logic operable to generate a negative representation of said subtrahend operand prior to routing to said address generation logic (see above regarding claim 12).

21. Regarding claim 14, Applicant discloses the data processing apparatus of claim 1, wherein said address generation logic comprises: operand generation logic operable to receive a first operand (X) associated with said instruction (see page 4, lines 13-14) and to generate a shifted operand representative of said first operand (multiplexer 130 generates shifted operand; see above regarding claim 1) shifted by a predetermined number of bits

(Note that the number of bits is determined when the code is written and before it is executed and is therefore predetermined.);

operand selection logic (multiplexer 130) operable, in dependence on said instruction, to select one of said first operand and said shifted operand (see page 3, lines 13-23) as a selected operand; and addition logic operable to add a second operand associated with said instruction to said selected operand (see page 3, lines 23-24) to generate said address for subsequent processing by said pipelined stages (memory stage 100; see page 1, last line; page 2, first line).

22. Regarding claim 15, Applicant discloses the data processing apparatus of claim 14, wherein said first operand comprises `n`-bits, where `n` is a positive integer (32; see page 3, lines 18-19), said operand generation logic receives said first operand (see page 3, lines 13-18) over an `n`-bit input bus (a bus used to transfer 32 bits is a 32-bit bus) and provides said shifted operand on an `n`-bit output bus (see page 3, lines 15-18;

Note that if an instruction needs to be shifted, the shifted value is eventually output from the multiplexer 130.),

said operand generation logic comprising: interconnection logic (multiplexer 130) operable to couple lines of the `n`-bit input bus with lines of the `n`-bit output bus to perform the shift operation (the multiplexer shifts data from the input bus to the output bus;

Note that the definition of the word shift according to The American Heritage® Dictionary of the English Language, Fourth Edition is "To move or transfer from one

place or position to another." Using this definition, the data is shifted from the input of the multiplexer to the output.).

23. Regarding claim 16, Applicant discloses the data processing apparatus of claim 14, wherein said operand selection logic is a two-input multiplexer (multiplexer 130, see fig. 4).

24. Regarding claim 17, Applicant discloses the data processing apparatus of claim 14, wherein said operand selection logic is operable to select one of said first operand and said shifted operand as a selected operand in response to a selection signal generated by instruction decoder logic (see page 3, lines 15-18;

Note that depending on the instruction, the multiplexer 130 can choose either the shifted operand, or the operand as an output instead of the inverse.).

25. Regarding claim 18, Applicant discloses the data processing apparatus of claim 14, wherein said addition logic is a two-operand adder (see fig. 4; page 3, lines 23-24).

26. Regarding claim 19, Applicant discloses the data processing apparatus of claim 1, wherein said operand routing logic is operable to route operands in response to a routing signal generated by instruction decoder logic

(Note that there must be a signal to control multiplexer 130. Whatever creates this signal is considered to be part of the decoder logic.).

27. Regarding claim 20, Applicant discloses the data processing apparatus of claim 1, wherein said instruction is a subtraction instruction which causes the processor core to generate said address by subtracting a subtrahend operand in the form of an immediate from a minuend operand (instruction a; see page 2, lines 18-20;

Note that if a negative integer is used as I, the instruction will subtract the positive number from register Rb),

and said data processing apparatus comprises instruction decoder logic operable to provide said subtrahend operand in negative form (see page 3, lines 13-14) to said address generation stage (X can be supplied to multiplexer 130, see page 3, lines 14-15) and to generate a routing signal to cause said operand routing logic to route operands to said address generation logic (see above regarding claim 19).

28. Regarding claim 21, Applicant discloses the data processing apparatus of claim 1, wherein said instruction is one of a load instruction (see page 3, line 16) and a store instruction.

29. Regarding claims 23-42, these claims recite equivalent limitations as claims 2-21 and are rejected under the same grounds.

Response to Arguments

30. Applicant's arguments filed 7 July 2006 have been fully considered but they are not persuasive.

Regarding the argument that the claims are subject to 35 U.S.C. §112 sixth paragraph, Examiner disagrees. The following is a quotation from the MPEP section 2181 [R-3]:

> [A] claim element that does not include the phrase "means for" or "step for" will not be considered to invoke 35 U.S.C. 112, sixth paragraph. If an applicant wishes to have the claim limitation treated under 35 U.S.C. 112, sixth paragraph, applicant must either: (A) amend the claim to include the phrase "means for" or "step for" in accordance with these guidelines; or (B) show that even though the phrase "means for" or "step for" is not used, the claim limitation is written as a function to be performed and does not recite sufficient structure, material, or acts which would preclude application of 35 U.S.C. 112, sixth paragraph.

Applicant has not amended the claims to include the phrase "means for" or shown that the current language of the claim does not recite sufficient structure, material or acts. On the contrary, Applicant states "the claim positively recites the corresponding structure which performs the claimed functions" (see remarks; page 16, 3rd paragraph). Further, the claims recite numerous limitations on the structure of the means which Applicant argues are subject to 35 U.S.C. §112 sixth paragraph. One example of such language is the term "logic" (lines 7 and 12 of currently amended Claim 1). The computer science definition of "logic" according to *The American Heritage® Dictionary of the English Language, Fourth Edition* is "Computer circuitry". This limitation adds certain physical structure to the limitation and therefore invalidates the use of 35 U.S.C. §112 sixth paragraph.

Examiner further asserts that the elements of Claim 22 do not invoke 35 U.S.C. §112 sixth paragraph for the same reasons. Mainly, the limitations do not use the term "step for".

31. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., specific structure used to shift operands and "enanabl[ing] one particular shift and add operation to be performed as fast as possible") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

32. Regarding the argument that the rejection under 35 USC §102 is based on three entirely different address generation arrangements, Examiner disagrees. Examiner based the rejection on the embodiment shown in figure 5. As applicant has shown in figures 4 and 5, the shift unit 160 and add unit 170 are equivalent in figures 4 and 5 (both have same reference number). Figure 4 is used merely because it shows the inner workings of the two units. It is also stated (page 4, lines 22-30) that the embodiment in figure 5 only differs from figure 4 in that the operands can be routed to bypass the shifter. Additionally, figure 3 is only referred to due to the greater detail disclosed. The other embodiments also receive operands X and Y, and can add

together register Y and shifted register X. Fig. 4 shows an improvement to the embodiment of Fig. 3 and Fig. 5 shows an improvement to Fig. 4.

33. Regarding the arguments that Figure 5 "fails to disclose the address generation logic as set out in claim 1 for the same reasons noted above", Examiner disagrees. As stated in the previous Office Action, Examiner pointed out where every limitation of Claim 1 could be found in the prior art. Address generation logic can be interpreted as logic which is used to generate addresses. The ADD unit of figure 5 is used in the address generation process and therefore can be interpreted as address generation logic. Regarding the argument that "adder 140 in Figure 4 simply performs an add without any shift operation", as Claim 1 states: "address generation logic... for generating a shifted operand". Claim 1 does not express that the operand must be shifted by the address generation logic. As stated in the previous Office Action, the shifted operand is generated by multiplexer 130, but is shifted prior to entry into the ADD unit.

Conclusion

34. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse R. Moll whose telephone number is (571)272-2703. The examiner can normally be reached on M-F 9:00 am - 5:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on 571-272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jesse R Moll
Examiner
Art Unit 2181

JM 9/25/06

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9/27/2006